REMARKS

The Office Action dated March 30, 2004, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

First, Applicants respectfully assert that the Office Action of March 30, 2004, was improvidently made final. While the Office Action alleges that "Applicant's submission of an information disclosure statement under 37 C.F.R. §1.97(c) with fee set forth in 37 C.F.R. §1.17(p) on 12/15/03 prompted the new ground(s) of rejection presented in this Office Action," Applicants note that the Information Disclosure Statement was NOT submitted *with a fee*, but rather with a *statement under 37 C.F.R. §1.97(e)*. As discussed in M.P.E.P. 609(B)(2)(i), "[i]f information submitted during the period set forth in 37 CFR §1.97(c) with a statement under 37 CFR §1.97(e) is used in a new ground of rejection on unamended claims, the next Office action *will not be made final* since in this situation it is clear that applicant has submitted the information to the Office promptly after it has become known and the information is being submitted prior to a final determination on patentability by the Office."

Because claims 11-23 were not amended in Applicant's Amendment filed February 9, 2004, and those claims were newly rejected over newly cited prior art in the Office Action of March 30, 2004 (Paper #9), the Office Action should not have been made final. Withdrawal of the finality of the last Office Action is respectfully requested.

Claims 1-7 and 11 were rejected under 35 USC § 102(e) as being anticipated by *Roy et al.* (WO 00/52858). Claims 8-10, 12-19 and 21-23 were rejected under 35 USC §

102(e) as being unpatentable over *Roy et al.* in view of *Simmons et al.* (U.S. Patent No. 6,084,856). Applicants note that claim 20 *was not rejected over prior art* although claims dependent thereon were rejected. Applicants respectfully requests clarification of the status of claim 20. Applicants respectfully submit that the presently pending claims recite subject matter which is neither disclosed nor suggested in the cited prior art.

The present invention is directed to, according to claim 1, a method of flow control management of data packets is disclosed. The method includes the steps of determining each time data is being written to memory in order to calculate a memory used amount, determining each time data is being freed from memory in order to calculate a memory freed amount, calculating how much total memory is being used using the memory freed amount and the memory used amount and comparing the total memory being used to a first predetermined threshold, wherein when the first predetermined threshold is reached a first threshold command is issued indicating that the first predetermined threshold has been reached and wherein the memory is implemented as a linked list, with pointers pointing to next memory locations in the linked list and the determining steps are performed when at least one of the pointers is moved.

The present invention is also directed to, according to claim 11, a method of flow control management of data packets is disclosed. The method includes the steps of determining a memory address to which a start pointer is pointing, wherein the start pointer points to a next memory location in a linked list to be read from memory, determining a memory address to which an end of list pointer is pointing, wherein the end

of list pointer points to a last memory location in the linked list, calculating from the start pointer and the end of list pointer a number of memory addresses which are being used by the linked list to determine a total amount of memory being used and comparing the total amount of memory being used to a first predetermined threshold, wherein when the first predetermined threshold is reached a first threshold command is issued indicating that the first predetermined threshold has been reached.

The present invention is directed to, according to claim 15, a switch. The switch includes a bus, a memory interface connected to the bus and to a memory, a receive port connected to the bus, the receive port receiving data packets for transmission to the memory through the bus and the memory interface, a transmit port connected to the bus, the transmit port transmitting data packets from the memory through the transmit port out of the switch and a flow control manager connected to the bus. The flow control manager includes a bus monitor that determines when the data packets are being transmitted to the memory and when the data packets are being transmitted from the memory to the transmit port, a counter that is incremented each time data packets are transmitted to the memory and decremented each time data packets are transmitted from the memory to the transmit port, wherein the counter indicates a memory being used value and a first comparator that compares the counter to a first predetermined threshold, wherein when the counter meets the first predetermined threshold a first threshold command is transmitted across the bus. The memory is implemented as a linked list, with pointers pointing to next memory locations in the linked list.

The present invention is directed to, according to claim 20, a switch. The switch includes a bus, a memory interface connected to the bus and to a memory, a receive port connected to the bus, the receive port receiving data packets for transmission to the memory through the bus and the memory interface, a transmit port connected to the bus, the transmit port transmitting data packets from the memory through the transmit port out of the switch and a flow control manager connected to the bus. The flow control manager includes a start pointer determiner that determines a memory address to which a start pointer is pointing to, wherein the start pointer points to the next memory location in a linked list to be read from memory, a end of list pointer determiner that determines a memory address to which an end of list pointer is pointing, wherein the end of list pointer points to the last memory location in the linked list, a memory used calculator that determines how many memory addresses are being used by the link list to determine a total amount of memory being used and a first comparator that compares the total amount of memory being used to a first predetermined threshold, wherein when the total amount of memory being used meets the first predetermined threshold a first threshold command is transmitted across the bus.

As discussed in the present specification, the present invention enables the flow of data packets in a network switch. Given that data packets can vary in size because they can have differently sized payloads, it is important to measure *the amount of memory used to store packets* rather than merely *the number of packets*. That is to say, measuring the number of variously sized packets in a queue does not access what percentage of the

queue is full without taking into account the sizes of those packets. Applicants respectfully assert that the prior art fails to provide the critical and unobvious advantages discussed above.

Roy et al. is directed to methods for managing multiple queues of *ATM cells* in shared RAM while efficiently supporting multicasting. Cells entering the switch are examined, placed in shared RAM, and a pointer to the RAM location is written in another location in the shared RAM. Table entries in management RAM are updated each time a cell is added to a queue. When a pointer exits a queue, the cell pointed to by the pointer is read and transmitted to the address of the queue. As the cell is read, the destination count for the cell is decremented. When the destination count is reduced to zero, the RAM location used to store the cell is added to the free list. Each time a pointer is read, the table entry for the affected queue is updated. When the queue becomes empty, an active bit in the table entry is toggled.

Applicants wish to emphasize that *Roy et al.* is directed to a method and apparatus for managing multiple *ATM cell queues*. Independent claims 1, 11, 15 and 20 all directed to methods and apparatuses for flow control management of *data packets*. Applicants also note that *Roy et al.* does not disclose any method or apparatus for handling data packets, as opposed to ATM cells. While it could be argued that the handling of the different data structures could be analogous, Applicants respectfully assert that *Roy et al.* fails to disclose all of the elements of the independent claims.

Claims 1 and 11 each recites, in part, a "method of flow control management of data packets," and claims 15 and 20 each recites, in part, "each receive port receiving data packets for transmission." "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully assert that *Roy et al.* fails to disclose all of the elements of claims 1, 11, 15 and 20, that the anticipation rejection over *Roy et al.* is improper and that the rejection should be withdrawn.

Similarly, Applicants also respectfully that the independent claims are not obvious in view of *Roy et al.* Because *Roy et al.* is directed to handling of ATM cells, as discussed above, *Roy et al.* is concerned only with the number of cells in a queue and not to the total memory being used. *Roy et al.* discloses, at page 7, lines 6 and 7, "a queue limit which indicates the maximum number of cells permitted in the queue." It is not clear that one of ordinary skill in the art would have been motivated to modify the system in *Roy et al.* such that it doesn't merely count cells but instead calculates how much memory is being used. The methodology would need to be modified to take into account the variable sizes of packets and there is not motivation to make such a modification. Thus, Applicants respectfully assert that the independent claims 1, 11, 15 and 20 would also not be obvious in view of *Roy et al.*

With respect to the rejections of 8-10, 12-19 and 21-23, deficiencies of *Roy et al.* were acknowledged and *Simmons et al.* was also cited. *Simmons et al.* is directed to a

network having a shared memory architecture for storing data frames has a set of programmable thresholds that specify when flow control should be initiated on full-duplex network ports. Flow control is initiated based on the number of available frame pointers by transmitting a PAUSE frame having a selected PAUSE interval to a transmitting network station. Specifically, a full-duplex port will output a PAUSE frame having a short, medium, or long programmed pause interval if the free buffer pool of available frame pointers falls below a high, medium, or low programmable threshold, respectively. The switch generates variable-length PAUSE control frames to minimize wasting network bandwidth.

Applicants respectfully assert that the combination of *Roy et al.* and *Simmons et al.* is improper because the motivation proffered for their combination is insufficient in view of disclosures of *Roy et al.* and *Simmons et al.* As noted above, *Roy et al.* is directed to controlling the flow of ATM cells and is unconcerned with having multiple thresholds. *Roy et al.* details only that cells are discarded, step 136, Fig. 9 of *Roy et al.*, and provides no basis for incorporating control frames, as discussed in *Simmons et al.* In other words, *Roy et al.* has no need for the processes disclosed in *Simmons et al.* and one of ordinary skill in the art would not have been motivated to combine the two references.

Additionally, Applicants respectfully assert that the rejection is guided merely by impermissible hindsight reasoning. "To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner show a motivation to combine the references that create the case of obviousness. In other words,

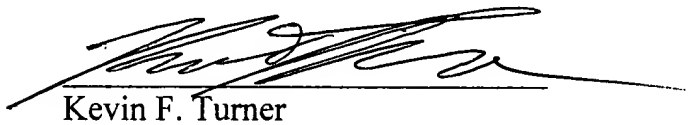
the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." In re Rouffet, 47 USPQ2d 1453 at 1458(CAFC 1998).

In view of the above, Applicants respectfully submit that claims 1, 11, 15 and 20 each recite subject matter which is neither disclosed nor suggested in a combination of *Roy et al.* and *Simmons et al.*, taken alone or in combination, and should be allowed. Similarly, claims 2-10, 12-14, 16-19 and 21-23 should also be allowed for at least their dependence on the independent claims. It is therefore respectfully requested that all of claims 1-23 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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